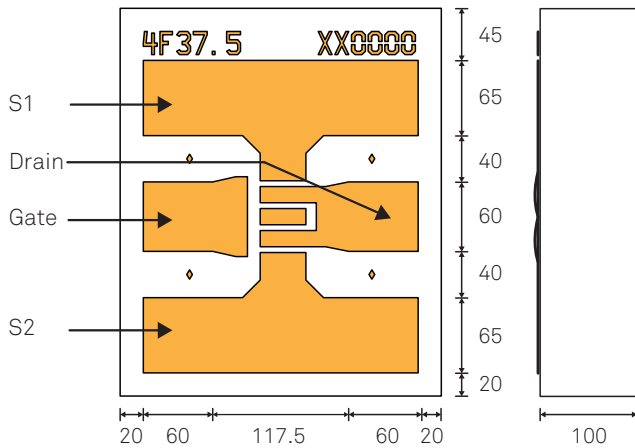


## 4 x 37.5 $\mu\text{m}$ Ultra Low Noise InP pHEMT

The pH-100 series of discrete ultra low noise InP HEMT transistors come in various standard sizes ranging from 50 $\mu\text{m}$  to 400 $\mu\text{m}$  total gate width. All transistors are DC-tested before shipment and have a unique label to allow for full traceability. In general it is best to use smaller devices at higher frequencies and larger devices at lower frequencies. Applications at room temperature often benefit from devices with more but shorter fingers, whereas 2-finger devices are usually optimal for applications at cryogenic temperatures.

The pH-100-4F37.5 with 150 $\mu\text{m}$  total gate width is typically used for hybrid LNAs covering frequency ranges from X-band up to Ku-band. Use in other frequency bands is possible and may make sense in cases with special requirements.



All dimensions are in micrometer.

### Basic Characteristics

Temperature	300 K
Transconductance $g_m$	1250 mS/mm
Maximum Drain Current $I_{DS\text{max}}$	800 mA/mm
Noise Figure $NF_{\text{min}}$ (@4 GHz)	0.12 dB
Noise Temperature $T_{\text{min}}$ (@4 GHz)	8 K
Associated Gain (@4 GHz)	22.7 dB
Noise Figure $NF_{\text{min}}$ (@30 GHz)	0.81 dB
Noise Temperature $T_{\text{min}}$ (@30 GHz)	60 K
Associated Gain (@30 GHz)	12.1 dB

### Typical Bias Range

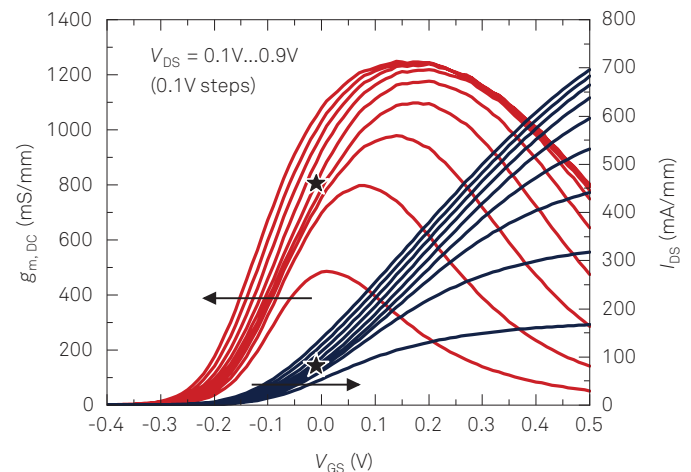
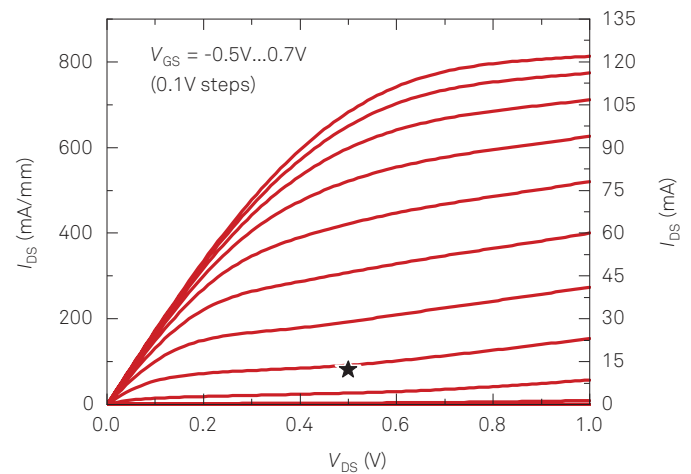
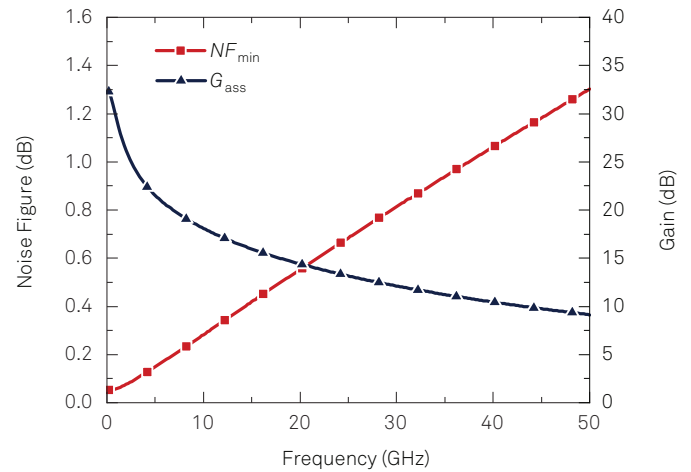
$V_{DS} = 0.2 \text{ V} \dots 0.75 \text{ V}$   
 $I_{DS} = 20 \text{ mA/mm} \dots 400 \text{ mA/mm}$   
 (3 mA ... 60 mA)  
 $V_{GS} = -0.2 \text{ V} \dots 0.25 \text{ V}$

### Maximum Ratings

$V_{DS} = 1.5 \text{ V}$   
 $V_{GD} = -2.5 \text{ V} \dots 0.5 \text{ V}$   
 $V_{GS} = -1.0 \text{ V} \dots 0.9 \text{ V}$

### Die Attach Notes

- Maximum die attach temperature is 200 °C
- It is recommended to use conductive epoxy
- Gold bond wires with diameter of  $\leq 25 \mu\text{m}$  are recommended
- Both source pads (S1, S2) need to be grounded
- To prevent damage to the active area in the center of the die avoid contact to this area during handling



★ denotes the typical low noise bias point of  $V_{DS} = 0.5 \text{ V}$  and  $I_{DS} = 80 \text{ mA/mm}$  (12 mA). The noise figure and gain plot is given for this bias and was obtained from on-wafer measurements.

Data and models are available on request.