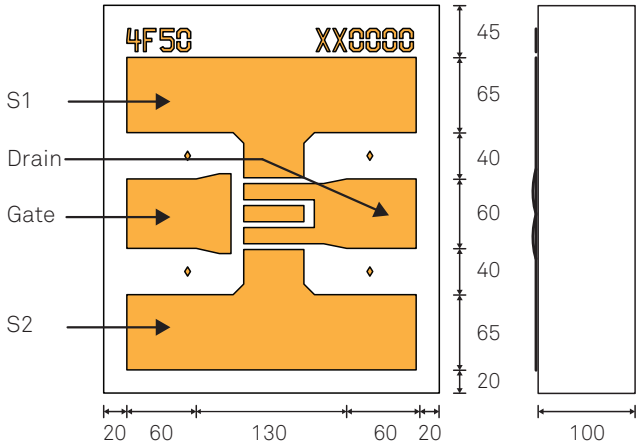
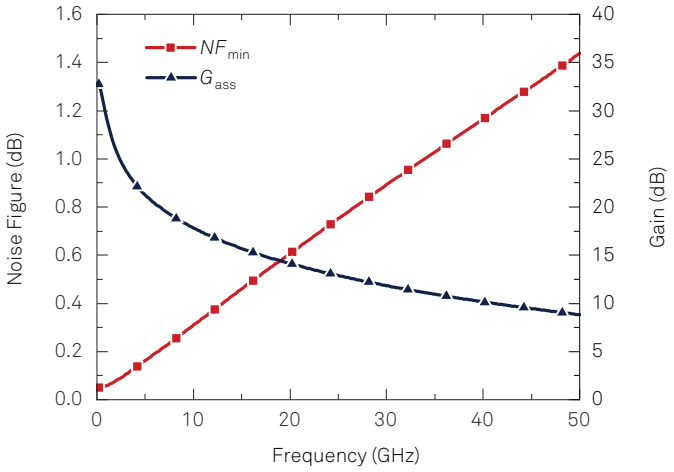
4 x 50 µm Ultra Low Noise InP pHEMT

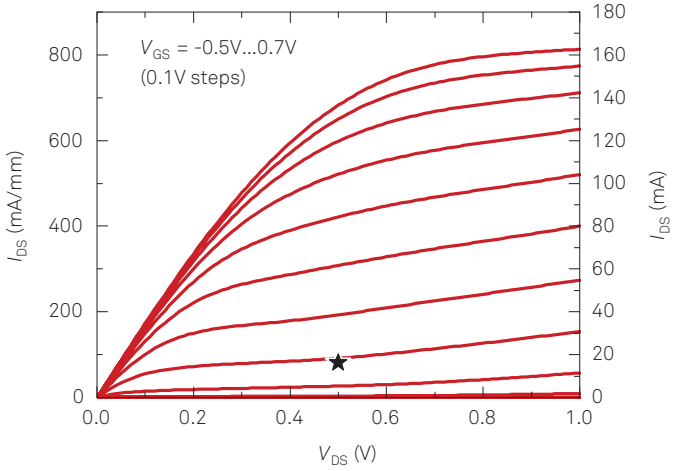
The pH-100 series of discrete ultra low noise InP HEMT transistors come in various standard sizes ranging from 50µm to 400µm total gate width. All transistors are DC-tested before shipment and have a unique label to allow for full traceability. In general it is best to use smaller devices at higher frequencies and larger devices at lower frequencies. Applications at room temperature often benefit from devices with more but shorter fingers, whereas 2-finger devices are usually optimal for applications at cryogenic temperatures.

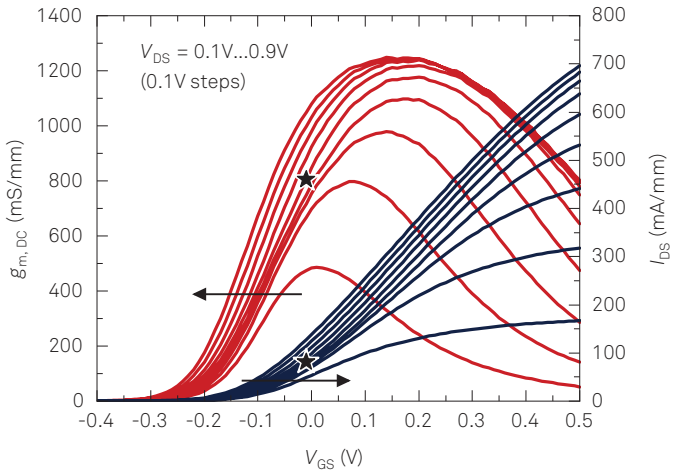
The pH-100-4F50 with 200µm total gate width is typically used for hybrid LNAs covering frequency ranges from L-band up to C-band. Use in other frequency bands is possible and may make sense in cases with special requirements.



All dimensions are in micrometer.







★ *denotes the typical low noise bias point of V_{DS} = 0.5 V and I_{DS} = 80mA/mm (16 mA). The noise figure and gain plot is given for this bias and was obtained from on-wafer measurements.*

Data and models are available on request.

Basic Characteristics

Temperature	**300 K**
Transconductance *gm*	1250 mS/mm
Maximum Drain Current I_{DSmax}	800 mA/mm
Noise Figure NF_{min} (@4 GHz)	0.13 dB
Noise Temperature T_{min} (@4 GHz)	9 K
Associated Gain (@4 GHz)	22.4 dB
Noise Figure NF_{min} (@30 GHz)	0.89 dB
Noise Temperature T_{min} (@30 GHz)	66 K
Associated Gain (@30 GHz)	11.8 dB

Typical Bias Range

V_{DS} = 0.2 V ... 0.75 V

I_{DS} = 20 mA/mm ... 400 mA/mm
(4 mA ... 80 mA)

V_{GS} = -0.2 V ... 0.25 V

Maximum Ratings

V_{DS} = 1.5 V

V_{GD} = -2.5 V ... 0.5 V

V_{GS} = -1.0 V ... 0.9 V

Die Attach Notes

- Maximum die attach temperature is 200 °C
- It is recommended to use conductive epoxy
- Gold bond wires with diameter of ≤ 25 µm are recommended
- Both source pads (S1, S2) need to be grounded
- To prevent damage to the active area in the center of the die avoid contact to this area during handling